CLAIMS

I claim:

1. An LDMOS transistor, comprising:

a body region of a first conductivity type formed in a semiconductor layer of a second conductivity type;

a source region of the second conductivity type formed in the body region;

a conductive gate insulated from the semiconductor layer by a first dielectric layer and overlying the body region, the source region being formed self-aligned to a first edge of the conductive gate;

an alignment structure formed adjacent a second edge, opposite the first edge, of the conductive gate, the alignment structure having a first edge in proximity to the second edge of the conductive gate and a second edge opposite the first edge; and

a drain region of the second conductivity type formed in the semiconductor layer self-aligned to the second edge of the alignment structure.

2. The LDMOS transistor of claim 1, wherein the conductive gate comprises a first polysilicon layer and the alignment structure comprises a second polysilicon layer, the second polysilicon layer being formed after the first polysilicon layer and being insulated from the first polysilicon layer by a second dielectric layer.

3. The LDMOS transistor of claim 2, wherein the first edge of the alignment structure overlaps the second edge of the conductive gate.

4. The LDMOS transistor of claim 2, wherein the second polysilicon layer comprises a heavily doped polysilicon layer.

5. The LDMOS transistor of claim 2, wherein the second polysilicon layer comprises a lightly doped polysilicon layer.

6. The LDMOS transistor of claim 1, wherein the alignment structure comprises a first polysilicon layer and the conductive gate comprises a second polysilicon layer, the second polysilicon layer being formed after the first polysilicon layer and being insulated from the first polysilicon layer by a second dielectric layer.

7. The LDMOS transistor of claim 6, wherein the second edge of the conductive gate overlaps the first edge of the alignment structure.

8. The LDMOS transistor of claim 6, wherein the first polysilicon layer comprises a heavily doped polysilicon layer.

9. The LDMOS transistor of claim 6, wherein the first polysilicon layer comprises a lightly doped polysilicon layer.

10. The LDMOS transistor of claim 1, wherein the conductive gate comprises a polysilicon layer and the alignment structure comprises a second dielectric layer.

11. The LDMOS transistor of claim 10, wherein the second dielectric layer comprises a silicon nitride layer.

12. The LDMOS transistor of claim 1, wherein the alignment structure is electrically shorted to the drain region.

13. The LDMOS transistor of claim 12, further comprising:

a drain contact opening formed above the drain region, the drain contact opening partially overlying the second edge of the alignment structure; and

a drain metallization formed in the drain contact opening, the drain metallization electrically connected to the alignment structure and to the drain region.

14. The LDMOS transistor of claim 1, further comprising:

a drain contact opening formed above the drain region; and

a drain metallization formed in the drain contact opening;

wherein the alignment structure is electrically isolated from the drain metallization and the drain region.

15. The LDMOS transistor of claim 1, further comprising:

a first region of the second conductivity type formed in the semiconductor layer and being more heavily doped than the semiconductor layer,

wherein the drain region is formed in the first region and the first region has a first edge proximate to an edge of the body region.

16. The LDMOS transistor of claim 15, wherein the first region abuts the body region.

17. The LDMOS transistor of claim 1, wherein the alignment structure is insulated from the semiconductor layer by a second dielectric layer.

18. The LDMOS transistor of claim 17, wherein a thickness of the first dielectric layer is different than a thickness of the second dielectric layer.

19. The LDMOS transistor of claim 1, wherein the alignment structure is formed on a top surface of the semiconductor layer.

20. The LDMOS transistor of claim 19, wherein the alignment structure comprises a heavily doped polysilicon layer.

21. The LDMOS transistor of claim 1, wherein the first conductivity type is P-type and the second conductivity type is N-type.

22. The LDMOS transistor of claim 1, wherein the first conductivity type is N-type and the second conductivity type is P-type.

23. The LDMOS transistor of claim 1, wherein the semiconductor layer comprises a well region of the second conductivity type formed in an epitaxial layer.

24. The LDMOS transistor of claim 1, wherein the body region is formed self-aligned to the first edge of the conductive gate.

25. The LDMOS transistor of claim 1, wherein the body region comprises a well region of the first conductivity type and is formed not self-aligned to the first edge of the conductive gate.

26. An LDMOS transistor, comprising:

a body region of a first conductivity type formed in a semiconductor layer of a second conductivity type;

a source region of the second conductivity type formed in the body region;

a conductive gate insulated from the semiconductor layer by a first dielectric layer and overlying the body region, the source region being formed self-aligned to a first edge of the conductive gate;

an alignment structure formed adjacent a second edge, opposite the first edge, of the conductive gate, the alignment structure having a first edge in proximity to the second edge of the conductive gate and a second edge opposite the first edge; and

a drain region of the second conductivity type formed in the semiconductor layer underneath the alignment structure.

27. The LDMOS transistor of claim 26, wherein the alignment structure comprises a heavily doped polysilicon layer and is formed on the surface of the semiconductor layer.

28. The LDMOS transistor of claim 27, wherein the drain region is formed by doping of the semiconductor layer by the alignment structure.

29. The LDMOS transistor of claim 27, further comprising:

a drain contact opening formed above the alignment structure, the drain contact opening being positioned above the drain region; and

a drain metallization formed in the drain contact opening, the drain metallization electrically connected to the alignment structure.

30. The LDMOS transistor of claim 27, wherein the conductive gate comprises a first polysilicon layer and the alignment structure comprises a second polysilicon layer, the second polysilicon layer being formed after the first polysilicon layer and being insulated from the first polysilicon layer by a second dielectric layer.

31. The LDMOS transistor of claim 27, wherein the alignment structure comprises a first polysilicon layer and the conductive gate comprises a second polysilicon layer, the second polysilicon layer being formed after the first polysilicon layer and being insulated from the first polysilicon layer by a second dielectric layer.

32. The LDMOS transistor of claim 26, wherein the drain region abuts the body region.

33. The LDMOS transistor of claim 26, wherein the first conductivity type is P-type and the second conductivity type is N-type.

34. The LDMOS transistor of claim 26, wherein the first conductivity type is N-type and the second conductivity type is P-type.

35. The LDMOS transistor of claim 26, wherein the semiconductor layer comprises a well region of the second conductivity type formed in an epitaxial layer.

36. An array of LDMOS transistors, comprising:

a first LDMOS transistor comprising:

a body region of a first conductivity type formed in a semiconductor layer of a second conductivity type;

a source region of the second conductivity type formed in the body region;

a conductive gate insulated from the semiconductor layer by a first dielectric layer and overlying the body region, the source region being formed self-aligned to a first edge of the conductive gate;

an alignment structure formed adjacent a second edge, opposite the first edge, of the conductive gate, the alignment structure having a first edge in proximity to the second edge of the conductive gate and a second edge opposite the first edge; and

a drain region of the second conductivity type formed in the semiconductor layer self-aligned to the second edge of the alignment structure; and

a second LDMOS transistor comprising:

a body region of a first conductivity type formed in a semiconductor layer of a second conductivity type;

a source region of the second conductivity type formed in the body region;

a conductive gate insulated from the semiconductor layer by a first dielectric layer and overlying the body region, the source region being formed self-aligned to a first edge of the conductive gate;

an alignment structure formed adjacent a second edge, opposite the first edge, of the conductive gate, the alignment structure having a first edge in

proximity to the second edge of the conductive gate and a second edge opposite the first edge; and

a drain region of the second conductivity type formed in the semiconductor layer self-aligned to the second edge of the alignment structure;

wherein the drain region of the first LDMOS transistor and the drain region of the second LDMOS transistor comprise a common drain region.